Amendments to the Claims

1. (Currently Amended) A method ~~in a memory having a bad memory cell, the method~~ comprising:

testing ~~the~~ a memory to determine ~~the~~ a location of ~~the~~ a bad memory cell;

mapping out an address location associated with the bad memory cell; and

offsetting ~~the~~ one or more physical address locations associated with one or more good memory cells so that logical addressing is linear and the memory appears contiguous.

2. (Original) The method of claim 1, wherein

the memory is within an integrated circuit and the testing is self-testing performed on chip by a built in self tester.

3. (Currently Amended) The method of claim 1, wherein

the memory is organized into one or more clusters, each of the one or more clusters having one or more memory blocks, and

~~the~~ mapping out of the address location associated with the bad memory cell includes mapping~~s~~ out a memory block having the bad memory cell.

4. (Currently Amended) The method of claim 3, wherein

~~the~~ offsetting ~~of the~~ one or more physical address locations associated with the one or more ~~of~~ good memory cells is by one memory block corresponding to the size of addressable space of the memory block having the bad memory cell.

5. (Currently Amended) The method of claim 4, wherein

each of the one or more good memory ~~block~~ cells, addressable in ascending order after the memory block having the bad memory cell, has its one or more physical address locations offset by the size of addressable space in a memory block to linearize the logical addressing.

6. (Currently Amended) The method of claim 3, wherein

there are four clusters ~~having~~ each having four memory blocks and each memory block contains 512 kilobits of memory cells.

7. (Currently Amended) The method of claim 1, wherein

~~the~~ testing the memory includes

writinges one or more test patterns into memory cells in the memory,

readings out data from the memory cells, and

comparinges the read out data with ~~the~~ an expected pattern of the one or more test patterns to determine ~~the~~ a location of the bad memory cell.

8. (Original) The method of claim 7, wherein

the location of the bad memory cell is associated with an address.

9. (Currently Amended) The method of claim 1, wherein

the memory is organized into one or more clusters, each of the one or more clusters having one or more memory blocks,

one or more bad memory cells are located within one or more respective memory blocks, and

~~the~~ mapping out ~~of~~ the address location includes mappings out the one or more respective memory blocks having the one or more bad memory cells.

10. (Currently Amended) The method of claim 9, wherein

~~the~~ offsetting ~~of~~ the one or more physical address locations ~~of~~ associated with the one or more good memory cells is by one or more memory blocks associated with the number of one or more respective memory blocks having the one or more bad memory cells and the corresponding size of addressable space of the memory block.

11. (Currently Amended) A reconfigurable memory comprising:

an array of memory cells; and

a reconfigurable memory controller to receive a logical address and generate a physical address to address the array of memory cells, the reconfigurable memory controller to map out one or more physical addresses of words having one or more bad memory cells to form a linear logical address space without addresses to words of the one or more bad memory cells.

12. (Currently Amended) The reconfigurable memory of claim 11, wherein~~,~~

the array of memory cells is organized into one or more clusters, each of the one or more clusters having one or more memory blocks.

13. (Currently Amended) The reconfigurable memory of claim 12, wherein~~,~~

the reconfigurable memory controller maps out ~~the~~ one or more physical addresses of memory blocks having the one or more bad memory cells.

14. (Currently Amended) The reconfigurable memory of claim 13, wherein~~,~~

the reconfigurable memory controller includes a configuration register associated with each memory block, each configuration register including ~~an~~ memory block enable bit, the memory block enable bit to map out the respective memory blocks having the bad memory cells.

15. (Currently Amended) The reconfigurable memory of claim 14, ~~wherein,~~

each configuration register further includes a base address associated with one or more upper address bits of an address to begin the physical addressing of a respective memory block having all good memory cells.

16. (Currently Amended) The reconfigurable memory of claim 15, ~~wherein,~~

~~the~~ a value of the base address is compared with ~~the~~ a value of the one or more upper address bits of the address to determine if each memory block having all good memory cells is selected for access.

17. (Currently Amended) The reconfigurable memory of claim 16, ~~wherein,~~

for a given memory block the comparison between the value of the base address and the value of the one or more upper address bits of the address results in a match and the given memory block is selected for access.

18. (Currently Amended) The reconfigurable memory of claim ~~1~~2, ~~wherein,~~

each memory block is a self contained memory unit including an array of memory cells, an address decoder, sense amplifier array and tri-state data bus drivers.

19. (Currently Amended) An integrated circuit comprising:

a reconfigurable memory ~~including~~ comprising:

an array of memory cells, and

a reconfigurable memory controller to receive a logical address and generate a physical address to address the array of memory cells, the reconfigurable memory controller to map out physical addresses of words having bad memory cells to form a linear logical address space without addresses to words of the bad memory cells.

20. (Currently Amended) The integrated circuit of claim 19, wherein,

the array of memory cells is organized into one or more clusters, each of the one or more clusters having one or more memory blocks.

21. (Currently Amended) The integrated circuit of claim 19, wherein,

the reconfigurable memory controller ~~of the reconfigurable memory~~ maps out ~~the~~ one or more physical addresses of one or more memory blocks having bad memory cells.

22. (Currently Amended) The integrated circuit of claim ~~19~~ 20, wherein,

the reconfigurable memory controller includes a configuration register associated with each of the one or more memory blocks, each configuration register including a memory block enable bit, the memory block enable bit to map out the respective memory blocks having the bad memory cells.

23. (Currently Amended) The integrated circuit of claim 19, wherein,

the reconfigurable memory controller includes a memory block base address.

24. (Original) The integrated circuit of claim 19, wherein

the integrated circuit is an application specific integrated circuit.

25. (Original) The integrated circuit of claim 24 further comprising:

a host port.

26. (Original) The integrated circuit of claim 24 further comprising:

a memory test register; and

a built-in memory self-tester.

27. (Original) The integrated circuit of claim 24 further comprising:

a memory test register;

a built-in memory self-tester; and

a test access port.

28. (Original) The integrated circuit of claim 24 further comprising:

a host port;

a memory test register; and

a built-in memory self-tester.

29. (Original) A method of conserving power in an integrated circuit having parallel data buses, the method comprising:

providing a bus keeper for each data bus in parallel together, the bus keeper to selectively keep the state of the bits of the respective data bus;

addressing one of the bus keepers to select a new data input to change the state on a selected data bus; and

maintaining the state on unselected data buses in parallel with the selected data bus to conserve power.

30. (Original) The method of claim 29, wherein,

power is conserved by avoiding the discharging of bit lines having charged parasitic capacitance in each unselected data bus and by avoiding the charging of bit lines having discharged parasitic capacitance in each unselected data bus.